Dawei Xu

+86 13469677955 | xudawei2005@zju.edu.cn | irqxm2le@gmail
davidsweb.top | xudawei42
Hangzhou, Zhejiang - 310007, China

Objective

Highly motivated junior student from Chu Kochen Honors College, Zhejiang University, with a solid foundation in computer systems and architecture and strong interests in network and architecture. Seeking a **Remote Research Internship** chances, with the ultimate goal of pursuing a **Ph.D. degree** starting in Fall 2027.

Education

- **Zhejiang University** *Sep. 2023 - Jun. 2027 (Expected)*
  B.Eng. in Computer Science and Technology Hangzhou, China
  - Chu Kochen Honors College
  - GPA: 3.72/4.0 (85.86/100)
  - Selected Core Coursework: Operating System (96), Computer Architecture (94), Computer and Logic Design Fundamentals (91), Computer Network (90), Object Oriented Programming (92)

Projects

- **Concurrent Command-line Chat Appllication over TCP** *Winter 2025*
  Tools: C++, Socket API [Code]
  - Built a concurrency server using C++ and Socket API, leveraging a multi-threaded thread-pool model to handle simultaneous client connections.
  - Defined and implemented a custom application-layer protocol to handle packet framing, preventing issues such as "sticky packets".
  - Utilized mutexes and semaphores to ensure thread safety and data consistency in shared message queues.
- **Developing a Unix-like Micro-Kernel** *Winter 2025*
  Tools: C, RISC-V Assembly, openSBI [*Code Private due to University Policy*]
  - Designed and implemented a multi-tasking kernel supporting Virtual Memory Management with Sv39 scheme, Process Scheduling using Round-Robin scheduler and System Call from user mode.
  - Implemented a FAT32 file system for persistent storage and a ELF loader for user-space programs execution.
- **Pipelined RISC-V Processor Design** *Spring 2025*
  Tools: Verilog, Vivado [*Code Private due to University Policy*]
  - Constructed a 5-stage pipelined CPU supporting the RV32I instruction set from the ground up, featuring hardware hazard detection and data forwarding.
  - Implemented a Speculative Execution mechanism with a Predict-Not-Taken strategy.
  - Extended the ISA to partially support Machine-mode Exceptions and Interrupts.
- **TCP/IP Protocol Stack Implementation (same as CS144 libsponge)** *Winter 2025*
  Tools: C++ [*Code Private due to University Policy*]
  - Designed a robust TCP Receiver capable of handling out-of-order, overlapping, and duplicate segments via a stream reassembler and cumulative acknowledgments.
  - Integrated components into a full TCPConnection, implementing a Finite State Machine to handle the three-way handshake and connection teardown.
  - Simulated routing logic for a functional IPv4 router.

Skills

- **Programming Languages:** C, C++, Python, Verilog, RISC-V Assembly

Honors and Awards

- **Second-class Scholarship** *2024-2025*
  Zhejiang University

References

1. **Kai Bu**
   Associate Professor, College of Computer Science and Technology
   Zhejiang University
   Email: kaibu@zju.edu.cn
   Relationship: Advisor